

STATUS AND PERSPECTIVE OF INDUSTRIAL TOPCON SOLAR CELL DEVELOPMENT AT FRAUNHOFER ISE

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ABSTRACT: This work reports on the status of industrial TOPCon solar cell development at Fraunhofer ISE. The baseline process makes use of Cz-Si:P wafers of M2 size, a TOPCon stack consisting of a thermal silicon oxide layer in combination with an 80 nm thin in-situ phosphorous-doped low-pressure chemical vapor deposited polysilicon layer as well as screen printed metal contacts. A comparison between different technologies for deposition of aluminum oxide (AlO_x) layers reveals advantages for atomic layer deposition, which considerably reduces minority carrier surface recombination, and as a result leads to an overall increase in solar cell efficiency. Potential challenges in contacting by screen-printed and fired silver contacts, which might arise due to the presence of an AlO_x layer on the rear side, are overcome by implementation of a laser-enhanced contact formation step, which reduces the series resistance of such solar cells by more than $2 \Omega\text{cm}^2$. These modifications of our baseline process in combination with a new generation of metallization pastes allows for the fabrication of solar cells with a champion efficiency of 23.8%. Our stable baseline process allows for evaluation of other TOPCon-related technologies or plated contacts, as well as identifying challenges for so-called TOPCoRE solar cells.

Keywords: TOPCon, Silicon Solar Cell, Manufacturing and Processing, Passivation

1 INTRODUCTION

More than 30 years passed between the initial presentation of the passivated emitter and rear cell (PERC) [1] and the actual large-scale manufacturing of that solar cell type. While the producers keep striving to push solar cell efficiencies, PERC is approaching its practical peak efficiency, however, due to physical limits of the cell architecture.

To keep up the learning rate of an increase of the conversion efficiency of industrial solar cells of around 0.5% absolute per year [2], a reduced time from lab to fab is required. After less than 10 years that the tunnel oxide passivated contact (TOPCon) solar cell has been initially published [3], industrial TOPCon (i-TOPCon) solar cells have already entered large-scale manufacturing in several production lines [4,5].

TOPCon technology, here used as an abbreviation for high-temperature passivating contact technology in general, i.e., excluding heterojunction technology, has been subject to increased research by numerous companies and research bodies over the last years. TOPCon combines a very thin silicon oxide (SiO_x) layer with a doped silicon layer to allow for very low surface recombination and to minimize metal contact related recombination.

Several technologies for formation of the tunnel oxide layer have been investigated. The tunnel oxide layer is very thin, typically in the range of 1 nm to 2 nm, to allow an efficient majority carrier transport, whereas others use oxide layers over 2 nm thickness, which are then deliberately broken by annealing at higher temperatures [6]. In most cases, SiO_x layers are being used that are formed by e.g., thermal oxidation, wet chemical oxidation, gaseous oxidation, or deposited layers; but also other materials are being investigated.

On top of the tunnel oxide layer, polysilicon layers are deposited. For this purpose, several technologies are possible, among which are low pressure chemical vapor deposition (LPCVD) [5], atmospheric pressure CVD (APCVD) [7], plasma-enhanced CVD (PECVD) [3,8], or sputtering / physical vapor deposition (PVD) [9]. In addition, some approaches come along with in-situ doping of the layer, i.e. addition of a doping precursor during deposition, whereas other choose to dope the layers ex-situ

in a separate process step, such as e.g. POCl_3 diffusion [5]. Regardless of the doping type, most TOPCon routes require some sort of longer high-temperature treatment for crystallization/dopant activation and dopant drive-in, whereas some approaches have been reported to only require a short contact firing step [10].

In addition to shallow dopant profiles, hydrogen management can play an important role for low recombination on the TOPCon side, and different approaches have been recommended, such as $\text{Al}_2\text{O}_3/\text{SiN}_x:\text{H}$ or $\text{SiN}_x:\text{H}$ layers, hydrogenation by illumination and heating [4] or water vapor annealing [11].

In this paper, we will show the actual status of our research on i-TOPCon solar cells at Fraunhofer ISE, which is conducted mainly in our pilot line laboratory PV-TEC [12], which in the mean-time consists of two separate labs for front-end and back-end processing. All research is being performed using M2 sized wafers; however, we are in the process of upgrading our line to keep up with industry needs and be able to process wafers up to G12 size. In addition, we will also give an update on TOPCon Rear Emitter (TOPCoRE) solar cell technology.

2 SAMPLE PREPARATION

2.1 Solar cells

For solar cell fabrication, phosphorous-doped M2-sized Cz-Si wafers are used. Saw damage removal and random pyramid formation in alkaline solution represents the first process. Conventional tube furnace diffusion at atmospheric pressure using a BBr_3 liquid precursor forms the boron emitter [13] with a sheet resistance of around $110 \Omega/\text{sq}$. The unwanted rear emitter is removed by a single side borosilicate glass (BSG) layer removal step in an inline tool and a silicon removal step, both of which either in an inline system in acidic ambient, or alternatively in a combination of inline system for BSG removal and batch system in alkaline ambient. The targeted Si removal is 4 to 6 μm , which ensures an efficient isolation of the wafer edge. In both cases, the front BSG needs to be kept intact. The TOPCon stack, which consists of a thermally grown SiO_2 tunnel oxide layer and an in-

situ doped polysilicon layer, both formed subsequently in one process in a low-pressure chemical vapor deposition (LPCVD) tube. The addition of PH_3 during polysilicon deposition leads to an in-situ doping of the around 80 nm thick deposited silicon layer.

As the polysilicon layer is wanted solely on the rear side of the sample, the parasitically deposited layer on the front side needs to be removed. This is being accomplished by etching in fluorine gas (F_2) at atmospheric pressure (atmospheric dry etching, ADE) in an inline tool, which also removes the polysilicon at the edges of the wafers and ensures a very high shunt resistance and sufficient reverse bias stability [14]. Due to its high selectivity, the front BSG layers is not etched during ADE, it acts as an etch stop for F_2 gas. The BSG layer is removed however in the next process step in fluoric acid (HF) solution, followed by cleaning of the wafers and thermal annealing for dopant activation in the TOPCon layer. For front side passivation, the SiO_x layer, which is formed during annealing, is removed during wafer cleaning. Surface passivation is being realized by deposition of a AlO_x layer by atomic layer deposition (ALD) in single slot configuration in a tube furnace, a subsequent outgassing step in another tube furnace, and the deposition of $\text{SiN}_x\text{:H}$ layers on front and rear by plasma-enhance chemical vapor deposition (PECVD). Alternatively, the $\text{AlO}_x/\text{SiN}_y\text{:H}$ stack on the front side is deposited by PECVD. Contact formation is realized by single step screen printing of a commercial Ag paste on the rear side, a AgAl paste on the front side and contact firing in a conventional conveyor belt furnace, yielding bifacial solar cells. In our industrial cell tester, we include a laser-enhanced contact optimization (LECO) step [15]. Its effect on IV parameters will be described later in the paper.

The described baseline process features a high flexibility and enables the implementation of alternative processes, such as PECVD TOPCon deposition [16] or plated metallization [17].

2.2 Lifetime samples

As an extension to our solar cell experiments, we typically fabricate asymmetric lifetime samples, i.e., cells without metallization, i.e., $p^+/n/n^+$ structure, for determination of the open circuit voltage limit iV_{oc} . For assessing the recombination at the front side of the cells, symmetric lifetime samples with random pyramids as well as Boron emitter, i.e., $p^+/n/p^+$ structure, and $\text{AlO}_x/\text{SiN}_y\text{:H}$ passivation layers are used. The latter allow for extracting the dark saturation current density j_{0e} in high injection from quasi steady-state photoconductance (QSSPC) measurements by the slope method. Similarly, symmetric $j_{0,\text{rear}}$ rear side samples, i.e., $n^+/n/n^+$ structure, enable a better understanding of the recombination at the rear side of the sample.

3 EXPERIMENTAL RESULTS

3.1 LPCVD TOPCon

As mentioned above, our TOPCon layer consists of a thermally grown tunnel oxide layer and an in-situ doped LPCVD polysilicon layer of only 80 nm thickness, both formed during one process. To evaluate the dopant profile of our process, both within the polysilicon layer as well as the tail in the crystalline Si wafer, electro-chemical capacitance voltage (ECV) profiling has been used. The result of such a measurement is depicted in Figure 1,

performed after thermal activation of the layer. The polysilicon layer features a rather constant dopant concentration of $2 \cdot 10^{20} \text{ cm}^{-3}$, which allows for a low-ohmic contacting of this layer by screen-printed Ag pastes. Beyond the tunnel oxide layer, the carrier concentration decreases rapidly, leading to a shallow phosphorous tail in the wafer itself. Please note that no correction of the dopant profile depth has been performed, thus the tunnel oxide layer seems to be located at an etch depth of around 60 nm, instead of the actual position at around 80 nm depth. The dark saturation current density $j_{0,\text{rear,SDE}} = 4 \text{ fA/cm}^2$ at a planar alkaline etched surface and $j_{0,\text{rear,txt}} = 10 \text{ fA/cm}^2$ at an alkaline textured surface reveal a decent surface passivation quality of this layer. However, by further tailoring of the dopant profile, lower recombination values seem realistic.

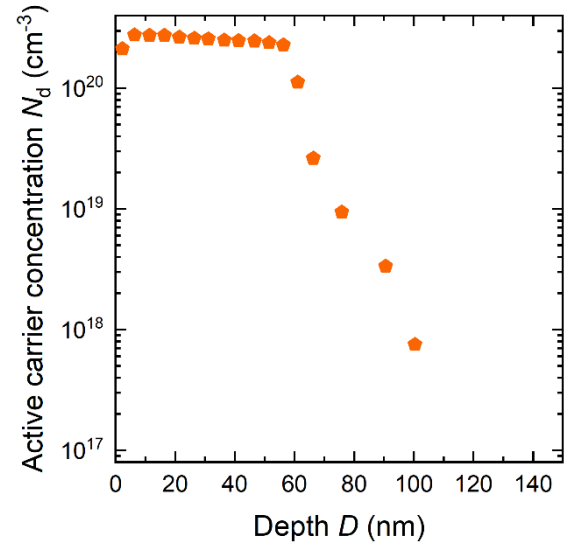


Figure 1: Active carrier dopant concentration N_d of a n-doped polysilicon layer, after thermal annealing, measured on a planar surface. Please note that no depth correction of the etched profile to a SEM thickness measurement has been performed.

One possible challenge for in-situ doped polysilicon layer deposition by LPCVD is the reduced deposition rate, when PH_3 gas is added for in-situ doping of the layer. To compensate this, often intrinsic layers are deposited, which are doped subsequently using POCl_3 diffusion furnaces (labelled “ex-situ doping”). Our results show that this approach yields similar recombination values $j_{0,\text{rear}}$ for planar and textured surfaces as the in-situ doping route.

As mentioned above, for the time being, LPCVD is our method of choice for i-TOPCon layer deposition. Two alternative methods for silicon layer deposition are PECVD and PVD. Both come with the potential advantages of strict single-sided deposition, which would eliminate the need for the one-sided polysilicon layer removal that is necessary for LPCVD layers [14]. While the PECVD process will be handled in the following section of this paper, there is a dedicated paper for the PVD route [18].

3.2 PECVD TOPCon

One significant challenge with direct-plasma PECVD of conductive layers can be the isolation of the electrodes. If the isolation is exposed to the plasma, as commonly the case for industrial direct-plasma PECVD tools, the isolation will be coated by deposition of conductive

phosphorus doped a-Si. This leads to a gradual shunting of the isolation and thus reduced process efficiency. Consequently, the deposition rate decreases until at some point the plasma collapses. In our case, when using a 24-wafer horizontal carrier, after approx. 3 to 4 deposition runs the carrier must be dismantled to replace the isolators. Therefore, we developed new isolators that can keep up the isolation even after multiple deposition runs with highly doped n-TOPCon. Figure 2 shows the determined deposition rate for 19 n-TOPCon process runs with the same process boat. The deposition rate is mostly stable and only shows some slight upwards trend, also influenced by the uncertainty in the thickness measurement on Cz wafers due to the rougher surface. Combined with a few depositions (not shown here), a total layer of approx. 9 μm thickness was deposited so far using the modified isolators.

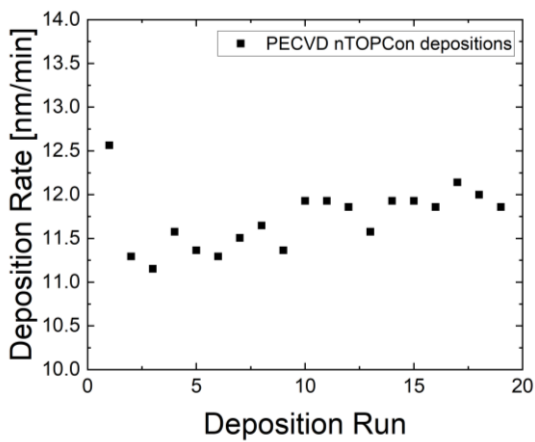


Figure 2: Deposition rate of PECVD n-TOPCon for 19 measured runs. Each deposition amounts to a thickness of 150 nm to 250 nm, depending on the target thickness. The total deposited thickness was approx. 9 μm .

3.3 Front side passivation

From around February 2020 until mid 2022, our boron emitter passivation was based on an $\text{AlO}_x/\text{SiN}_y:\text{H}$ stack, which has been deposited by PECVD. However, in mid 2022, we were able to setup a process for high throughput thermal, temporal ALD in a tube furnace batch system, and we compared this ALD process to our PECVD reference process. By putting one wafer in each slot of the ALD process boat, we chose to deposit Al_2O_3 on both sides of the samples of this group, which is achieved easily due to nature of double-sided deposition during the process. The results reveal that the ALD process reduced j_{0e} to 15 fA/cm^2 , compared to $j_{0e} = 24 \text{ fA}/\text{cm}^2$ for the PECVD passivation approach. This is in agreement with values shown by others [4,19] for similar dopant profiles, which yields an increase of the median implied V_{oc} of asymmetric cell precursors of around 4 mV, see Figure 3. Nevertheless, although the results already make hope for a positive transfer towards solar cells, it is mandatory to also fabricate such solar cells, as the possible existence of an Al_2O_3 layer on the rear side might negatively affect the contact formation between Ag paste and poly-Si layer. However, the metallization process (see next section) showed to be tolerant to the presence of the Al_2O_3 layer and the solar cell conversion efficiency increased by 0.5% absolute for the ALD route, because of a 6 mV higher V_{oc} and an increase in fill factor FF by 0.6% absolute. The different increase of iV_{oc} and V_{oc} hints towards another positive effect of the Al_2O_3 deposition on the rear side, and

in fact $\text{Al}_2\text{O}_3/\text{SiN}_x:\text{H}$ stacks on top of polysilicon layers have been reported to allow for an improved hydrogenation compared to single $\text{SiN}_y:\text{H}$ layers [20]. An alternative explanation might be that the existence of a thin Al_2O_3 layer on the rear side retards the contact formation and a thus lower $j_{0,\text{met}}$ would result in a higher V_{oc} . Further insight into that topic is necessary to determine the underlying effect and to be able to separate between the two explanations.

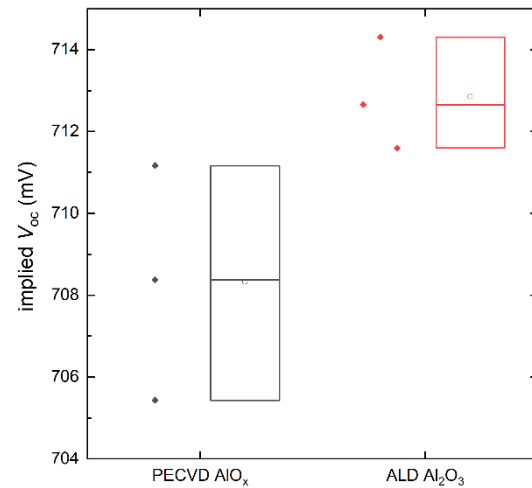


Figure 3: Implied open circuit voltage of asymmetric lifetime samples (non-metallized TOPCon cell precursor) for determination of the V_{oc} limit, measured after firing and illumination anneal.

3.4 Contact optimization

At Fraunhofer ISE, we implemented a laser enhanced contact formation (LECO) treatment into our cell tester. Explaining all the details of this LECO step is beyond the scope of this paper, but more information can be found in literature [21,22]. The LECO process allows for under-firing the contacts by reducing the required firing set temperature, which reduces the damage induced by the metal contact and thus e.g. $j_{0,\text{met}}$ at the front side [23]. In this case, LECO leads to a significant improvement in IV parameters. For our TOPCon solar cells, LECO leads to an increase of the conversion efficiency of up to 4% absolute (see Figure 4), by considerably reducing the average series resistance of the solar cells from 2.81 Ωcm^2 to 0.46 Ωcm^2 , which results in an increased fill factor. This LECO treatment is especially important in case of Al_2O_3 layers on the rear side, since these layers hinder contact formation for non-adapted Ag pastes, resulting in extremely low fill factors for such cells. In such cases, LECO can demonstrate its full potential. The overall champion solar cell treated with LECO and measured at our industrial cell tester is listed in Table 1.

Table 1: IV parameters extracted from measurements in an industrial cell tester, after LECO, using a GridTouchTM unit with 30 wires for current and 5 wires for voltage, and measured versus a black and electrically non-conductive background.

Poly Thickness	η (%)	j_{sc} (mA/cm^2)	V_{oc} (mV)	FF (%)
80 nm	23.5	40.7	706	81.7

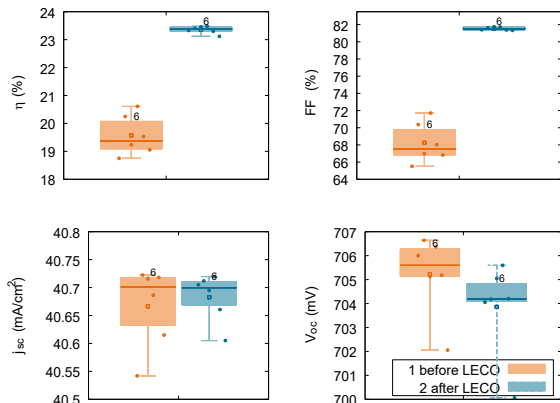


Figure 4: Impact of LECO processing on typical IV data, measured at an industrial cell tester.

Table 2 shows the IV parameters of another industrial M2 sized i-TOPCon solar cell from another run, which has been subject to a calibrated measurement at Fraunhofer ISE CalLab PV Cells, using a golden, reflective chuck and 30 current wires. The solar cell features $V_{oc} = 706$ mV, $j_{sc} = 41.3$ mA/cm², and $FF = 81.6\%$, which results in a conversion efficiency $\eta = 23.8\%$. As described above, the polysilicon thickness on the rear side is only 80 nm, as confirmed by scanning electron microscopy. The front side passivation consists of an ALD deposited Al₂O₃ layer in combination with a PECVD SiNx layer. Single step screen printing and single step firing form the metal contacts, followed by LECO treatment.

Table 2: IV parameters from our champion M2 solar cell with area 244.5 cm² and a polysilicon thickness of 80 nm (n-doped, in-situ). The calibrated measurement has been performed at Fraunhofer ISE CalLab on a golden reflective chuck with full area rear side contacting, using 30 wires for current and 5 wires for voltage, neglecting the grid resistance.

Status	η (%)	j_{sc} (mA/cm ²)	V_{oc} (mV)	FF (%)
As processed	23.8	41.3	706	81.6
After MgF ₂	24.0	41.6	708	81.6

3.5 TOPCon vs. TOPCoRE

So far, in all experiments described above, n-type Si wafers have been used. However, for reasons of cost and dopant segregation over the ingot, p-type Cz-Si wafers are still of relevance. In addition, Ga-doped Si-wafers feature a high minority carrier lifetime and are favorable to boron-doped Si wafers with respect to potential iron contamination. This makes them interesting for use in so-called TOPCoRE solar cells, i.e., a TOPCon solar cell, where instead of a n-type Si wafer, a p-type Si wafer is used. This transition puts the emitter on the rear side of the cell, in this case then a polysilicon passivated contact emitter, and the boron diffused front side becomes a front surface field, which due to the high conductivity of the wafer itself does not need to contribute to lateral conductivity and which can be thus optimized with respect to passivation quality and contact formation only. On the one hand, this cell structure is very sensitive to front side recombination and carrier diffusion length, as photogenerated electrons need to reach the cells rear side, and on the other hand to carrier recombination at the rear side metal contacts due to presence of the pn junction. A

possible too deep contact at the rear emitter side would lead to a direct shunting of the device.

So far, in few experiments, we used high quality, high-ohmic Ga-doped Cz-Si wafers for fabrication of such TOPCoRE solar cells. For reasons of stability, we increased the thickness of the polysilicon layer to 160 nm, however first tests with 80 nm of n-doped polysilicon were successful, too, and showed almost an identical conversion efficiency, with differences in the range of 0.1%. All other processes from the above-described process i-TOPCon sequence have been left unchanged. The measurements at Fraunhofer ISE CalLab PV Cells show an efficiency of 23.2% for such p-type TOPCoRE devices, which forms a promising starting point for further progress on such cells. More information on this cell structure can be found in the respective paper [24].

3.6 Plating

The combination of local laser ablation of passivation layers and a plated stack of nickel (≈ 0.5 μ m thickness) / copper (5 to 10 μ m) / silver (< 0.5 μ m) [25] offers the possibility to reduce more than 90% in silver consumption for industrial TOPCon solar cells. Furthermore, recent publications from Fraunhofer ISE [26] could demonstrate that low-damage laser contact opening for plating enables to further reduce the poly-Si thickness of the TOPCon contact down to 60 nm and by that further reduce processing cost of TOPCon solar cells.

Figure 5 shows the V_{oc} of industrial TOPCon precursors metallized with i) either both sides plated Ni/Cu/Ag or ii) screen-printed silver (no LECO) contacts on the poly-Si rear side, and screen-printed AgAl paste on the front side. The plated solar cells feature an increased V_{oc} of about 5 mV compared to the screen-printed reference. Photoluminescence imaging (PL) of test fields on i-TOPCon solar cell precursors with and without laser contact openings (LCO) on a sample with 60 nm poly-Si thickness demonstrate that the application of UV picosecond laser ablation yields a marginal laser-induced damage with an average iV_{oc} decrease of only 1 mV. These results show the potential to decrease the poly-Si thickness by introducing laser defined plated contacts for i-TOPCon solar cells. Furthermore, recent developments at Fraunhofer ISE [6] show that the contact resistivity ρ_c below 1 m Ω cm² allows to decrease the LCO width down to 5 μ m, which leads to plated contact widths of about 12 μ m only.

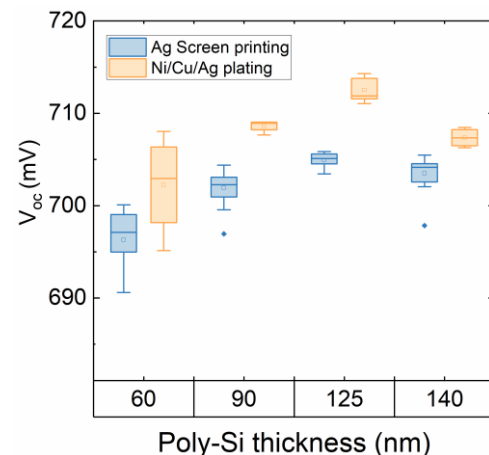


Figure 5: Measured V_{oc} of plated and screen printed TOPCon solar cells with variation of poly-Si thickness on the TOPCon rear side (from [26]).

The recent progress in reducing the impact of laser-induced damage in LCO improved contact resistivity and contact aspect ratio [17,27], which allowed to achieve champion solar cell efficiencies of 24% [26] (see Table 3) for industrial TOPCon solar cells with plated Ni/Cu/Ag contacts. The low-damage, narrow plating contacts allowed an improvement of 0.5% absolute compared to the screen-printed metallization at the R&D line of the cell supplier.

Table 3: Calibrated IV measurements of champion TOPCon solar cells (poly thickness: 125 nm) with plated or screen printed metallization measured at Fraunhofer ISE CalLab using industrial TOPCon precursors [26].

Metallization	η (%)	J_{sc} (mA/cm ²)	V_{oc} (mV)	FF (%)
Ag/AgAl screen printed (supplier, no LECO)	23.5	40.7	705	81.9
Plated Ni/Cu/Ag (FhG-ISE)	24.0	41.0	715	82.0

4 SUMMARY

In this paper, we have shown an overview over our activities in the field of i-TOPCon solar cells. Within a short time of only a few years, TOPCon technology has matured from a proof of concept to an industrial cell concept, which has already been transferred into production by many cell manufacturers. Several technologies are available for both interface oxide formation and polysilicon layer deposition, and while each of them seems to allow for a high quality TOPCon layer, in the end it might come down to questions like uptime, stability, process flow integration, and of course cost.

We have developed a process flow for i-TOPCon solar cells, which makes use of an in-situ doped polysilicon layer formed by LPCVD, with screen-printed metallization. Champion results are currently in the range of 24% for M2-sized Cz-Si:P wafers, with a polysilicon thickness of only 80 nm. Notable efficiency improvements have been achieved recently by the implementation of ALD AlOx deposition and LECO treatment. In addition, we plan to upgrade all relevant tools until end of 2023, to be able to process wafers up to G12 size.

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